TRIZ APPLICATION IN DEVICE & MANUFACTURING ELECTROSTATIC DISCHARGE CONTROL

Teong-San Yeoh
Intel Technology Sdn. Bhd.
Penang, Malaysia
ts.yeoh@intel.com

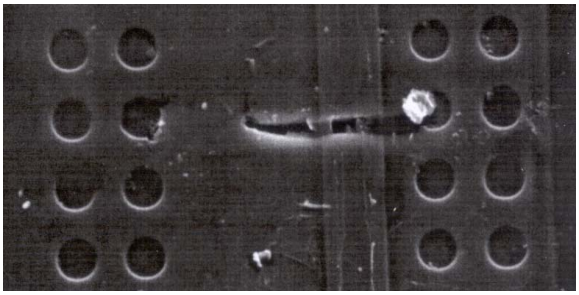
ABSTRACT

Electrostatic Discharge (ESD) is a common failure mechanism found in semiconductor device manufacturing. ESD can be generated from humans, machines or even during the handling of these semiconductor devices. This paper explores the application of TRIZ's Inventive Principles in device and manufacturing ESD Control. In device ESD, the key focus is on the design of the many different ESD protection structures used in the device protection scheme. Basically, ESD protection in the device is based on the Inventive Principles of *Skipping* and *Equipotentiality*. In terms of the design of the various ESD protection cells used in the device, the fundamental design of these cells relate to the Inventive Principles which includes *Curvature, Cushioning in Advance, Merging, Asymmetry, Segmentation, Universality, Taking out, Blessing in Disguise* and *Intermediary*. In manufacturing ESD, the Inventive Principles of *Preliminary Action, Composite Materials* and *Flexible Shells & Thin Films* are demonstrated. This is one of the first attempts to assess the Inventive Principles in the device design and manufacturing ESD controls. Since ESD can be extremely difficult to control in the manufacturing process, a deeper understanding of the Inventive Principles including their application will enable more robust designs and manufacturing controls for current and future process technologies.

INTRODUCTION

Electrostatic Discharge (ESD) is the rapid transfer of electrostatic charges between bodies of surfaces that are at different electrostatic potentials; and is a common failure mechanism for semiconductor devices. ESD damage is often caused by human handling of devices (Human Body Model) or robotic handling (Machine Model) during manufacturing. The devices themselves can also get charged during automated manufacturing and their discharge to ground causes damage (Charged Device Model). These failure mechanisms can be in the form of transistor gate oxide breakdown, transistor drain to source diffusion punchthrough (Figure 1) or charge trapping.

Figure 1: Transistor drain to source diffusion punchthrough due to ESD



The sources of ESD can be from humans, equipment or even during the handling, transportation or manufacturing process of these semiconductor devices. Due to the fabrication process technology trend towards smaller dimensions, the semiconductor device susceptibility of ESD is predicted to correspondingly worsen as shown in Figure 2 which is the ITRS (International Technology Roadmap for Semiconductors) roadmap.

Figure 2: ITRS 2002 roadmap

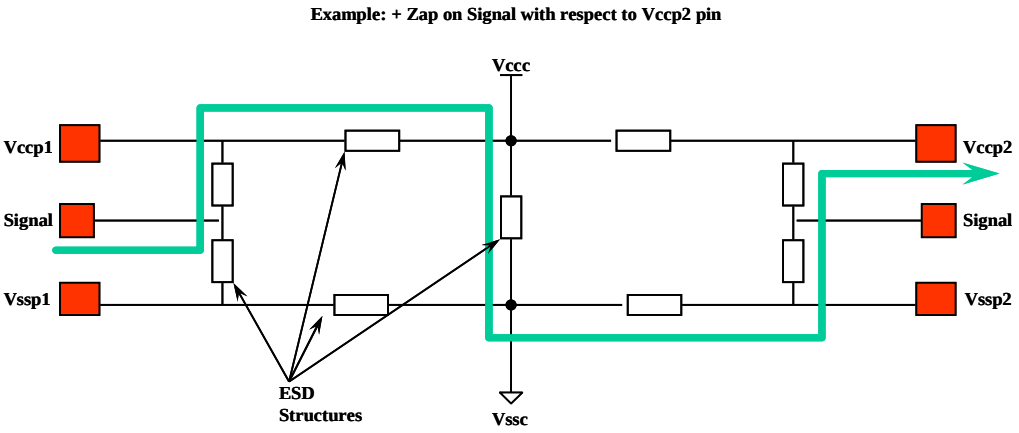
Year	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
Node	130nm	115nm	100nm	90nm	80nm	70nm	65nm	45nm	32nm	22nm
Maximum allowable static charge on devices	(100-250)V	(100-250)V	(100-250)V	100V	100V	50V	50V	25V	25V	10V

In order to address this projected worsening trend, device and manufacturing ESD controls need to be effectively implemented and be robust. This paper will address some of the standard ESD practices, along with its relationship to TRIZ's Inventive Principles. This will help assist future ESD controls to be hinged upon these Inventive Principles as guidance.

DEVICE ESD

In device ESD, the key focus is on the design of the many different ESD protection structures used in the device protection scheme. The main objective of the ESD protection structures is to be able to move short pulse (1-100ns), high ESD current (1-10 Amps) discharge from affected pin/ball/contact to the grounded part of the device in the shortest amount of time. Figure 3 shows the flow of the ESD current from Signal pin (input) to Vccp2 pin (output) via the various ESD structures inside the device.

Figure 3: ESD current discharge path from Signal pin to Vccp2 pin



Basically, ESD protection in the device is based on the Inventive Principles of *Skipping a.k.a. Rushing through/Hurrying* (Principle #21) where the ESD current flowing through the device needs to be moved at high speed to prevent heat buildup which would then damage the internal components of the device. The ESD structures prevent damage to internal circuitry by providing a discharge path in case of an ESD event. This is

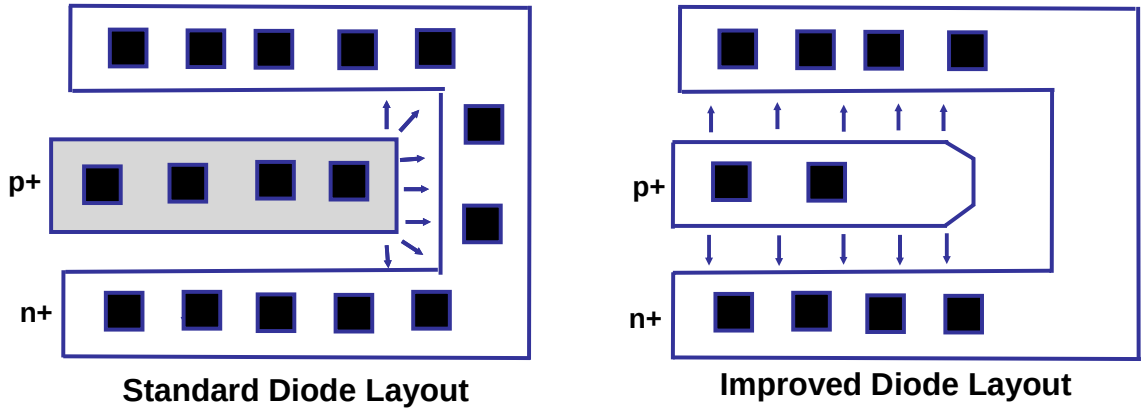
Cushioning in Advance which is Principle #11 (i.e. prepare emergency means beforehand to compensate for the relatively low reliability of an object). The other Inventive Principles which are demonstrated is *Equipotentiality* (Principle #12) where the potential difference between two bodies need to be equalized to prevent a charge transfer; and *Merging* (Principle #5) where similar ESD structures are repeated across the device to enable parallel ESD current discharge. These ESD structures are in the form of ESD power clamps for the power supply (Vcc) and ground (Vss) of the device, which are distributed evenly across the entire power ring in the device.

In terms of the design of the various ESD protection cells used in the device, the fundamental design of these cells relate to the Inventive Principles which include *Curvature, Merging, Asymmetry, Segmentation, Universality, Taking out, Blessing in Disguise* and *Intermediary*.

a) ESD Input Buffers

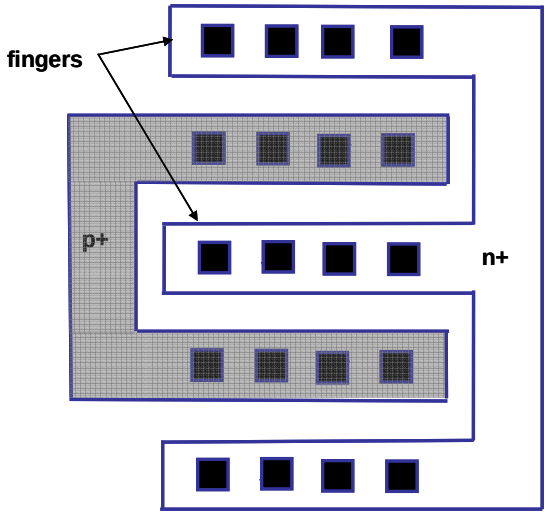
Figure 4 below shows a standard versus an improved diode layout for ESD input buffers. The sharp corner of the standard diode will result in a high field (Corona effect) at the edges which may potentially breakdown during an ESD event. Rounding the corners (*Curvature*, Principle #14) in the improved diode layout will prevent the high field effect. In addition, some of the contacts have been improved to reduce the high current concentration which is demonstration of *Asymmetry* (Principle #4).

Figure 4: Diode layout for Input buffer



Since these ESD structures are relatively large taking up precious silicon space due to need to be able to absorb the high ESD current flow, the need for long widths is segmented (*Segmentation*, Principle #1) into shorter multiple fingers which are more compact in area (Figure 5).

Figure 5: Diode layout with multiple fingers



b) ESD Input/Output and Output buffers

Figure 6 shows a typical n-channel transistor which operates under normal working conditions but transforms into an npn bipolar transistor during an ESD event. This is making a part perform multiple functions, thus eliminating the need for other parts i.e. *Universality a.k.a. Multi-functionality* (Principle #6). It can also be considered that the npn bipolar transistor separates an interfering part which is the ESD current i.e. *Taking out a.k.a. Extraction, Separation* (Principle #2). In order for the ESD current to be conducted through at low resistance, there must be many electron-hole pairs generated by impact ionization and current needs to reach avalanche breakdown. When a sufficiently large number of holes have been collected in the substrate, the parasitic bipolar transistor switches on and the drain current reaches the snapback region which offers a very low resistance to the ESD current (Figure 7). Although impact ionization is not desired in normal operation as it leads to avalanche breakdown, it is important for ESD current flow which is a high current with fast discharge time. This can be considered as *Blessing in disguise* (Principle #22)

Figure 6: npn bipolar transistor during ESD event

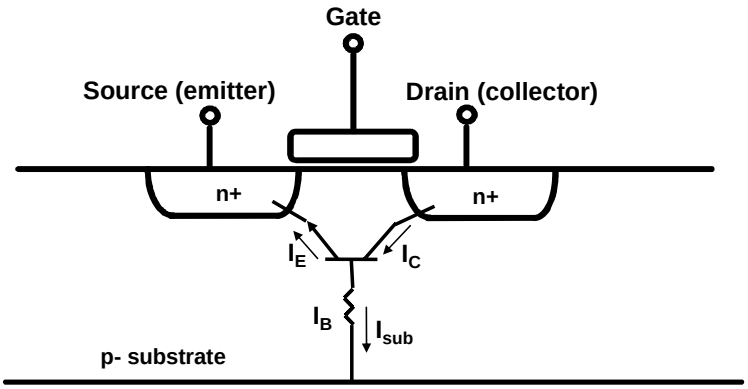
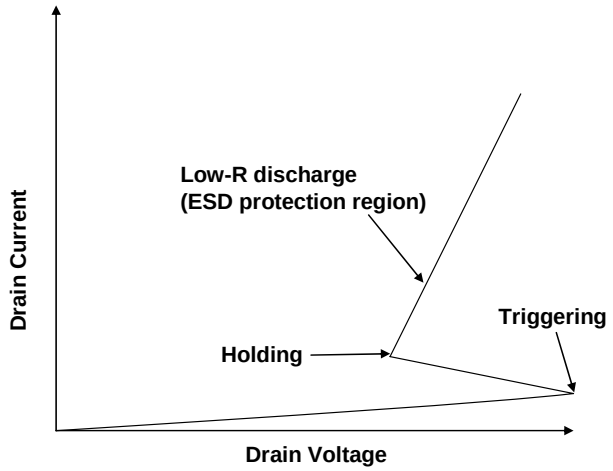
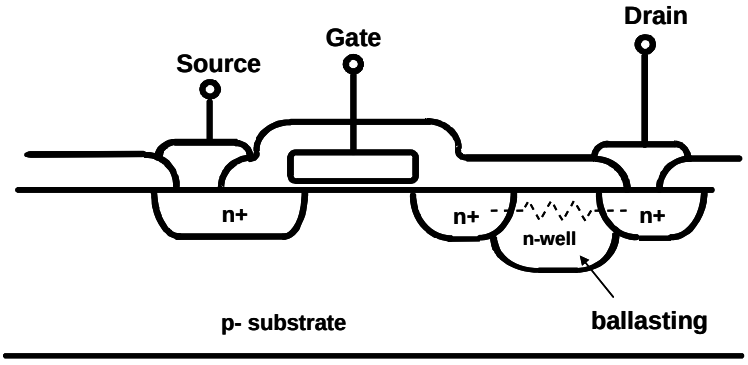


Figure 7: Snapback Current-Voltage characteristic



As for metal salicided fabrication processes, the source and drain diffusions are coupled with a layer of metal salicide which reduces the diffusion resistance significantly. This poses a problem as the high ESD current will not have sufficient time to evenly distribute across the diffusion contacts but will concentrate into only 1-2 contacts due to the lowered resistance. This will result in high temperature buildup in those contacts which then damages the ESD structure. In order to overcome this, n-well diffusions which have higher resistance values are inserted between drain diffusion and gate (*Intermediary*, Principle #24) to improve ballasting effect for salicided processes (Figure 8). Ballasting basically provides a means for ESD current to distribute more evenly across the drain contacts.

Figure 8: Cross-section of ESD structure with ballasting effect



These are just some examples of how the various Inventive Principles are being used in Device ESD. As for Manufacturing ESD, other Inventive Principles are utilized.

MANUFACTURING ESD

In manufacturing ESD, the key focus is on reducing or eliminating ESD potential or field induction buildup. Inventive Principles of *Preliminary Action, Composite Materials* and *Flexible Shells & Thin Films* are demonstrated.

a) Air ionizers

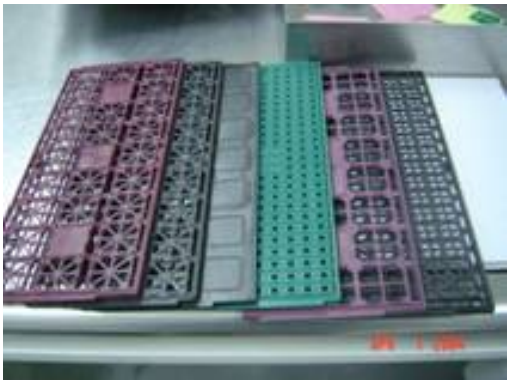
One of the equipment used to reduce ESD potential buildup is through the use of air ionizers (Figure 9) which is able provide high concentrations of positive and negative charged ions to neutralize any charged object in its proximity. This is applying *Preliminary Action* which is Principle #10 (i.e. perform before it is needed).

Figure 9: Air ionizer

b) Trays and carriers

In order to transport the semiconductor devices, the trays or carriers (Figure 10) need to be made of static dissipative material in order to slow down any rapid ESD discharge. This material is made of *Composite Material* (Principle #40) which has carbon or graphite filler in material such as Polyether Sulfone. Similarly, metal surfaces which directly contact the device are also coated with a similar dissipative material.

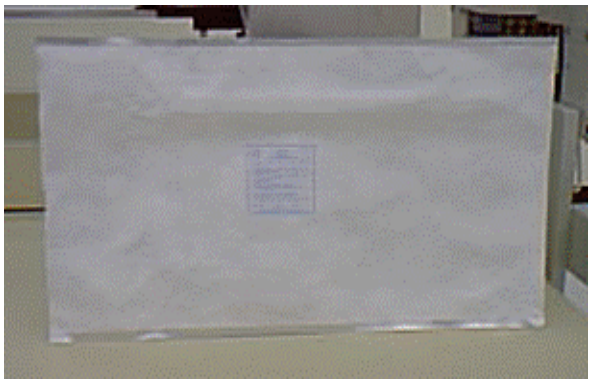
Figure 10: Static dissipative trays



c) Conductive Bags

During transportation, these semiconductor devices are also isolated from the external environment through the use of conductive bags (Figure 11). These bags provide a Faraday shield from any ESD source. This is *Flexible Shells and Thin Films* (Principle #30). Similarly, the cover tape for tape & reel is also demonstrating Principle #30.

Figure 11: Conductive bag



SUMMARY

Since ESD is a common failure mechanism in the semiconductor industry and will continue to be so in future due to the fabrication process technology trend, more effort is needed to study the current Device and Manufacturing ESD controls and how the Inventive Principles are being utilized. So far, the Inventive Principles of *Segmentation (#1), Taking out (#2), Asymmetry (#4), Merging (#5), Universality (#6), Preliminary Action (#10), Cushioning in Advance (#11), Equipotentiality (#12), Curvature (#14), Skipping(#21), Blessing in Disguise (#22), Intermediary (#24), Flexible Shells & Thin Films (#30), Composite Materials (#40)* have been observed. This is one of the first attempts to assess the Inventive Principles in the Device and Manufacturing ESD controls, including device design. Moving forward, a deeper understanding of how the Inventive Principles can be applied to future ESD controls will be even more important, including studies on TRIZ's Trends of Engineering System Evolution.

REFERENCES

1) Song, C.L., Choo, W.C., Yeoh, T.S., '*Emerging needs for test handler CDM ESD controls*', International Conference on Semiconductor Electronics Proceedings, pp 180, 2004.
2) Yeoh, T.S., '*Building in reliability during ESD design layout*', International Physical & Failure Analysis Symposium Proceedings, pp 172, 1997.
3) Altshuller, Genrich, '*40 Principles TRIZ Keys to Technical Innovation*', Technical Innovation Center, MA, 2002.
4) Tate, Karen and Domb, Ellen, *'How to Help TRIZ Begineers Succeed'*, TRIZ Journal, 1997.
5) Mann, D.L., '*Hands-On Systematic Innovation*', CREAX Press, Ieper, 2002.